**CSE 202: DIGTAL LOGIC DESIGN**

**Credit Hours:** 3

**Contact Hours:** 3

1. **COURSE OUTLINE**

Digital vs Analog, Binary digits, Logic levels and digital waveforms, Logic operation and functions, Switches and relays, Fundamental logic gates, Boolean Algebra and logic simplification, Fundamental theorems of Boolean Algebra, Truth tables, Karnaugh Map, SOP and POS minimization, Combinational circuits, Number systems, operations and codes, Design of various logic functions, e.g. Adders, Comparators, Encoders/Decoders, Mux/DeMux, BCD-to-7-Segment Decoder, Implementation of combinational circuits using discrete chips and programmable logic devices, i.e. ROMs/PLAs, Speed and delays in logic circuits, Sequential circuits, Latches, Flip-Flops and their applications, 555 Timer, Sequential circuit applications, Asynchronous and synchronous counters, UP/DN counters, Shift registers, Semiconductor memories, RAM, ROM, PROM and EEPROM, Flash memories, Design of a simple processor.

1. **WEEKLY PLAN**

|  |  |
| --- | --- |
| **Week** | **Contents** |
| Week 1 | 1. Digital vs. Analog 2. Binary Logic, Digital Logic Gates, and Digital Waveforms 3. Number Systems 4. Binary Codes |
| Week 2 | 1. Boolean Algebra 2. Fundamental Theorems of Boolean Algebra |
| Week 3 | 1. Digital Design Procedure    1. Problem Statement    2. Input-Output Relationship 2. Boolean Functions 3. Truth Tables 4. Boolean Expression 5. Canonical Form 6. Standard Form |
| Week 4 | 1. Simplification Techniques    1. Iterative Method    2. Karnaugh Map |
| Week 5 | 1. Common Logic Circuits Design Examples-I    1. Code Converters (BCD-to-Excess-3, BCD-to-7-segment)    2. Odd-Prime Detector    3. Magnitude Comparator    4. Parity Generator and Checker |
| Week 6 | 1. Common Logic Circuits Design Examples-II    1. Adders    2. Subtractors 2. Encoders 3. Decoders 4. Implementation of Logic Circuits using Decoders |
| Week 7 | 1. Multiplexers 2. Demultiplexers 3. Implementation of Logic Circuits using Multiplexers |
| Week 8 | 1. Concept of Memory    1. Read Only Memories (ROMs)    2. Programmable Logic Arrays (PLAs) 2. Implementation of combinational circuits using discrete chips and programmable logic devices, i.e. ROMs/PLAs |
|  | **Midterm Examination** |
| Week 9 | 1. Sequential circuits 2. Latches |
| Week 10 | 1. Flip-Flops and their applications    1. SR Flip-Flop    2. D Flip-Flop    3. JK Flip-Flop    4. T Flip-Flop |
| Week 11 | 1. Edge Triggered vs. Level Sensitive    1. JK Flip-Flop    2. Master Slave Flip-Flop 2. Sequential circuit applications    1. 1-bit Random Access Memory |
| Week 12 | 1. Registers    1. Buffer Registers    2. Shift Registers    3. Parallel to Serial Converters    4. Serial to Parallel Converters |
| Week 13 | 1. Design Procedure of Asynchronous/Ripple Counters    1. Up Counters 2. Down Counters 3. Up-Down Counters 4. Controlled Counters 5. Modulus Counters 6. Presettable Counters |
| Week 14 | 1. Design Procedure of Synchronous Counters 2. Ring Counters |
| Week 15 | 1. Hardware design of a simple Computer involving the following units    1. Program Counter    2. Memory Address Register    3. Random Access Memory    4. Instruction Register    5. Arithmetic Logic Unit    6. Temporary Registers    7. Controller Sequencer    8. Introduction to Assembly Language Programming using the Instruction Set of a Simple Microprocessor leading to 8085    9. Timing States & Instruction/Program Execution Time |
| Week 16 | Course Revision |
|  | Finalterm Examination |

1. **CLOs AND THEIR MAPPING WITH PLOs**

|  |  |  |  |
| --- | --- | --- | --- |
| **CLO**  **#** | **CLO** | **Level of Learning** | **PLOs** |
| **CLO-1** | Understand different number systems, binary addition and subtraction, 1’s and 2’s complement representation, addition and subtraction with these representations, Boolean algebra theorems and their applications to combinational logic circuits | Cog-3 (Application) | PLO-1 (Engineering Knowledge) |
| **CLO-2** | Translate descriptions of logical problems to digital logic circuits and define the Karnaugh map to perform an algorithmic reduction of logic circuits | Cog-4 (Analysis) | PLO-2 (Problem Analysis) |
| **CLO-3** | Design and understand the following combinational and sequential circuits: adders, subtractors, encoders, decoders, multiplexers, (de)multiplexers, parity generators, comparators, ROMs, PLAs, latches, flip-flops, counters, and shift registers; and to perform simple projects with them | Cog-5 (Synthesis) | PLO-3 (Design/Development of Solutions) |
| **CLO-4** | Integrate simple combinational and sequential circuits into a fairly large-scale system to meet specified requirements | Cog-5 (Synthesis) | PLO-3 (Design/Development of Solutions) |

1. **CLOs ASSESSMENT MECHANISIM**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Course Assessment Tools** | **CLOs** | | | |
| **CLO-1** | **CLO-2** | **CLO-3** | **CLO-4** |
| Assignments | 🗸 | 🗸 | 🗸 | 🗸 |
| Quizzes | 🗸 | 🗸 | 🗸 | 🗸 |
| Class participation | 🗸 | 🗸 | 🗸 | 🗸 |
| Midterm examination | 🗸 | 🗸 | 🗸 |  |
| Final term examination |  | 🗸 | 🗸 | 🗸 |

1. **MARKS DISTRIBUTION** (for conventional grading)

Final-term: 60 %

Midterm: 20 %

Sessional: 20 % as per following distribution:

Assignments: 10 %

Quizzes: 10 %

1. **RESOURCES**
   * TEXT BOOKS
     + Digital Design by Morris Mano
     + Digital Computer Electronics by Malvino & Brown
   * REFERENCE BOOKS
     + Digital Fundamentals by Thomas L. Floyd